

CLAIMS

What is claimed is:

1 1. A communication profiler, for use with a data processing system including a
2 processor and a memory coupled by a system interconnect, wherein said communication
3 profiler comprises:

4 a control unit including an input port coupled to said system interconnect,
5 wherein said control unit receives a collection of data via said input port as a result of a
6 tenure on said system interconnect, wherein said control unit filters said collection of
7 data from said tenure to obtain specific data requested by a user and organizes said
8 specific data as a summary.

2. The communication profiler according to claim 1, further comprising:

2 a profiler interconnect; and

3 a profiler memory, coupled to said profiler interconnect, wherein said profiler
4 memory stores said summary.

1 3. The communication profiler according to claim 1, further including:

2 an output port that can be coupled to an external analyzer to communicate said
3 summary.

1 4. The communication profiler according to claim 1, further comprising:

2 a control register, coupled to said control unit, which activates filtering of said
3 collection of data by said control unit.

1 5. The communication profiler according to claim 1, further including:

2 a transaction timer, coupled to said control unit, wherein said transaction timer
3 is utilized to record a duration of a operation pending.

1 6. The communication profiler according to claim 1, further comprising:

2 a data serializing and transmitting device that serially outputs said summary from
3 said communication profiler, wherein said summary is indicative of normal hardware
4 performance.

1 7. A data processing system, comprising:

2 a system interconnect;

3 a plurality of master elements, coupled to said system interconnect;

4 a plurality of slave elements, coupled to said system interconnect; and

5 a communication profiler, coupled to said system interconnect, further including:

6 a control unit including an input port coupled to said system interconnect,
7 wherein said control unit receives a collection of data via said input port as a result of a
8 tenure between a master element and a slave element on said system interconnect,

9 wherein said control unit filters said collection of data from said tenure and retrieves a
10 set of specific data requested by a user and organizes said set of specific data as a
11 summary.

1 8. The data processing system according to claim 7, wherein said data processing system
2 is a small computer system interface (SCSI) controller.

1 9. The data processing system according to claim 7, wherein said data processing system
2 is implemented on a single integrated circuit substrate.

1 10. A host data processing system comprising:

2 a host interconnect;

3 a host processor coupled to said host interconnect;

4 a host memory coupled to said host interconnect;

5 a data processing system including a processor and memory coupled by a system
6 interconnect comprising:

7 a plurality of master elements, coupled to said system interconnect;

8 a plurality of slave elements, coupled to said system interconnect; and

9 a communication profiler, coupled to said system interconnect, further
10 including:

11 a control unit including an input port coupled to said system
12 interconnect, wherein said control unit receives a collection of data via said input port
13 as a result of a tenure between a master element and a slave element on said system
14 interconnect, wherein said control unit filters said collection of data from said tenure and
15 retrieves a set of specific data requested by a user and organizes said set of specific data
16 as a summary.

11. The host data processing system according to claim 10, further comprising:

2 a memory controller, coupled to said host interconnect, utilized to control said
3 host memory.

1. A method for gathering hardware performance data, comprising the steps of:

2 activating a communication profiler coupled to a system interconnect by setting
3 a control register, coupled to a control unit in said communication profiler;

4 monitoring a system interconnect for a tenure between a master element and a
5 slave element of a data processing system; and

6 capturing a set of data resulting from said tenure and organizing said set of data
7 into a summary, in response to detecting a tenure on said system interconnect.

1 13. The method for gathering hardware performance data according to claim 12, further
2 comprising the step of:

3 deactivating said communication profiler, by resetting said control register.

1 14. The method for gathering hardware performance data according to claim 12, further
2 comprising the step of:

3 transmitting said summary to an external analyzer.